Request For Reconsideration

Claims 14-20 were rejected under 35 U.S.C. ¶102 as being anticipated by Graettinger et al. (US 6348709). Applicants respectfully traverse this rejection.

The Examiner's attention is directed to FIG. 2 of the present application. As recited in claim 14, an interlayer dielectric layer 15 is formed on a pad 13 and a substrate 11 so as to insulate the pad. Then, a bit line stack 23 is formed on the interlayer dielectric layer 15, and bit line spacers 25 are formed at side walls of the stack 23. A storage node contact hole is formed in the interlayer dielectric layer 15 using a self-aligned contact etching so as to expose the pad 13. Finally, as shown in subsequent figures, a contact plug is formed in the contact hole 26.

Graettinger et al. does not teach the aforementioned features of claim 14. That is, referring to FIG. 2 of Graettinger et al., the gate electrodes 120 are formed on an underlying substrate 110, not an interlayer dielectric layer. Further, if even the substrate 110 of Graettinger et al. were somehow considered an interlayer dielectric layer, there is no teaching in Graettinger et al. of self-aligned contact etching of a contact hole in an interlayer dielectric layer that is formed under a gate electrode stack.

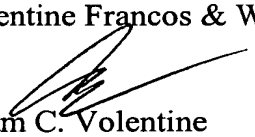
For at least the reasons stated above, Applicants respectfully contend that claims 14-20 are not anticipated by Graettinger et al.

Conclusion

No other issue remaining, reconsideration and favorable action upon the claims 14-20 now pending in the application are requested.

Respectfully submitted,

Volentine Francos & Whitt, PLLC



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